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(71) Applicant: APPLIED MATERIALS, INC. [US/US]; P.O. Box 450A, Santa Clara, CA 95052 (US).

(72) Inventors: CHABALA, Jan, M.; 408 Summer Creek Lane, San Ramon, CA 94583 (US). KRISHNASWAMI, Sriram; 1632 Nightingale Avenue, Sunnyvale, CA 94087 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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(54) Title: MULTIPASS PRINTING WITH INCREASED THROUGHPUT AND LITHOGRAPHIC QUALITY

(57) Abstract: A method for a raster scan particle or light beam lithography system for writing in multiple passes to form an effective writing grid that is larger than the input address size. The composite of all passes forms a staggered checkerboard pattern of overlapping pixels. The desired pattern is sampled using a sampling matrix having an array of cells, e.g., 8x8, of a predetermined input address size. Each pass produces a writing grid defined by the distance between beam placements in a single pass. The composite of all passes forms the effective writing grid. Thus, for example, a total of eight passes may be used to form eight offset writing grids. The resulting writing grids may be eight times the input address size, and effective writing grids may be twice the input address size. Consequently, throughput is increased. Moreover, the spot size produced by the particle or light beam may be at least approximately eight times the input address size to ensure good lithographic quality. Different sampling matrices may be used depending on whether there is a horizontal or vertical feature in the pattern being sampled of if the feature is at a particular angle.

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MULTIPASS PRINTING WITH INCREASED THROUGHPUT AND LITHOGRAPHIC QUALITY

Jan M. Chabala
Sriram Krishnaswami

FIELD OF THE INVENTION

The present invention relates to particle or light beam systems used in the manufacture of microminiature electronic devices (integrated circuits) and is particularly directed to a new and improved writing technique for raster scan beam lithography system.

BACKGROUND

It is well known to use particle (electron or ion) or light beam exposure systems for the manufacture of microminature electronic devices (integrated circuits). Often these systems use raster scan beam lithography methods. Such lithographic systems can employ a controllable electron beam, sometimes called E-beam machines, for the fabrication of integrated circuits. Such systems are well known, see for example, U.S. Patent 3,900,737 to Collier et al., U.S. Patent 3,801,792 to Lin, U.S. Patent 4,469,948 to Biechler et al., U.S. Patent 4,879,605 to Warkentin et al., U.S. Patent 5,103,101 to Berglund, and U.S. Patent 5,393,987 to Abboud et al. all of which are incorporated by reference.

In these machines a medium of resist (or photosensitive) material upon which the electron beam is to perform its writing operation is provided overlying a substrate which is to become a mask for imaging a wafer or which is the wafer itself (direct writing). The medium with its underlying substrate is positioned on a motor-driven stage which is moved continuously in synchronism as the beam is scanned in a raster fashion (a raster scan) and in a direction perpendicular to the stage motion. In practice, the diameter of the round electron beam spot, also called a "Gaussian spot" or "pixel", focussed on the resist layer, is of the order of (but not

necessarily equal to) the writing address dimension (or address unit) of the Cartesian grid on which it is written. Adjacent rows of pixels in the stage travel direction define the width of a "feature" and a height of the feature is formed by a number of pixels in the raster scan direction. The feature is for instance an element of the integrated circuit such as a conductive interconnect or a portion of a transistor. In practice, adjacent "on" pixels in the same raster scan are not separately scanned; instead the beam is kept on until an "off" pixel is encountered. For the purposes of this disclosure, descriptions are given in terms of the normal full pixelization representation, unless specifically discussed otherwise. The turning on and off of the beam is achieved by a beam blanker which is a well known portion of an E-beam machine, one example of which is shown in U.S. Pat. No. 5,276,330, entitled "High Accuracy Beam Blanker" incorporated by reference herein, invented by Mark A. Gesley. The pattern on the resist defined by the beam scan and by the stage movement is determined by the system control equipment, which includes certain computer software programs.

Prior art teaches that repetitive "multipass" imaging strategies for raster scanning lithographic systems are desirable. Repeated writing of scan lines placing pixels in nominally the same location has long been used to increase the dose of energy delivered to the patterned area on the substrate. The higher dose allows the use of less sensitive but higher resolution and/or higher contrast resist coatings for improved lithography. Additionally, the redundancy averages out some of the random errors in the lithographic system. Further improvement may be obtained by offsetting the data within the raster scan line so that the repeated image spots (pixels) are still written redundantly at nominally the same substrate location, but from a different portion of the scan line. Lithography is improved because of averaging of systematic errors of the lithographic system. This is described in "Image Quality Enhancements for Raster Scan Lithography", L. Rieger, et al, 1988 SPIE Santa Clara Symposium. With a conventional writing technique, throughput is disadvantageously reduced proportional to the number of passes required for the repetitive imaging.

Other pertinent art is disclosed in "Rasterizing System Utilizing An Overlay Of Bit-Mapped Low Address Resolution Databases" U.S. Patent 4,879,605 to Warkentin, et al. A multi-pass writing technique is disclosed which requires multiple edge definitions achieved by varying the dosage at an edge dependent upon the desired location of a given edge. With a normal raster scan writing technique, feature edges are logically defined in the obvious manner by a row of exposed or "on" pixels at the feature edge. Incorporation of nonhomogeneous edge definitions into the writing technique requires more stringent control over other lithographic system and image development parameters to make all edges appear alike and resolve to the proper location when the image is developed.

Other pertinent art is disclosed in "Multiphase Printing for E-Beam Lithography" U.S. Patent 5,103,101 to Berglund et al. A multi-pass writing technique interleaves pixels in a series of passes with each pass offset from others by a fraction of the writing address required to achieve the composite cartesian pixel array.

Another relevant disclosure is U.S. Pat. No. 4,498,010 to Biechler et al. which provides a virtual addressing technique and is incorporated by reference.

SUMMARY

The writing technique in accordance with the present invention is performed in a raster scanning particle beam or light beam lithography system. The final pixelization of the lithographic pattern on the substrate consists of overlapping pixels whose centers form a staggered checkerboard type pattern. Multipass printing achieves the desired pixelization using a series of offset passes, with each pass producing a writing grid. In one embodiment, eight passes are used. The multiple passes form superimposed writing grids to form an effective writing grid, i.e., the array defined by the beam placement on the mask surface after completion of all passes. The effective writing grid is larger than the individual address unit.

In accordance with an embodiment of the present invention, the desired pattern is sampled with a sampling matrix prior to printing. The sampling matrix includes an array of cells, e.g., an 8x8 array, with the size of each cell defining an input address unit. The effective writing grid is at least twice the size the input address size and each writing grid is eight times the size of the input address size. Consequently, throughput is increased over single pass printing or other forms of multipass printing, e.g., described in U.S. Patent 5,103,101. Moreover, the spot size produced by the particle or light beam may be varied, and may be at least approximately eight times the input address size to ensure good lithographic quality. The intensity of the particle or light beam may be varied to adjust the total energy (dose) delivered to the substrate, e.g., a mask or a wafer. Different sampling matrices may be used to sample the desired pattern depending on whether there is a horizontal or vertical feature in the pattern of if the feature edge is at an angle. If the feature is at an angle, different matrices may be used depending on the precise angle.

The present invention may be used with virtual addressing, as described in "Virtual Addressing for E-Beam Lithography", U.S. Patent 4,498,010 to Biechler et al. (incorporated herein by reference). In addition, offset scan voting may be used in accordance with the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a writing operation by a raster scan lithography machine in accordance with the present invention.

Fig. 2 illustrates a particle beam lithographic system.

Fig. 3 shows an input pattern grid with superimposed writing grid and effective writing grid, which is laid down in eight passes, used in accordance with an embodiment of the present invention.

Fig. 4 illustrates the writing strategy used in U.S. Patent 5,103,101 to Berglund et al.

Fig. 5 shows a sampling matrix for sampling pattern data with horizontal and/or vertical edges.

Fig. 6 shows four sampling matrices that may be used for angled edges.

Figs. 7, 8, 9A, 9B, and 10 illustrate the operation of sampling a geometric figure, storing the pattern data and printing the figure on a mask in accordance with an embodiment of the present invention.

Fig. 11 shows schematically offset scan voting (eight pass).

DETAILED DESCRIPTION

Fig. 1 illustrates a writing operation by a raster scan lithography machine in accordance with the present invention. As shown in Fig. 1, the arrow "X" represents the movement of the stage 10 and the arrow "Y" represents the movement of the electron beam or light beam in a single scan in written stripe 14. The arrow 12 represents the movement of the stage 10 in the Y axis direction after completing a written stripe 14. Each written stripe 14 is produced by a series of scan lines 16, e.g., up to 262144 scans lines 16. A scan line is the full length of the set of pixels (not shown in Fig. 1) that are sequentially placed on the mask surface 11 without interruption from the beam retrace 18. The scan line height depends on the address size and blanker rate, which will be discussed below. The scan line may be, for example, 8192 bits when the lithography system is operating at 320 MHz. Each pixel is an individual beam placement on the mask or wafer surface 11. As indicated in Fig. 1, multiple written stripes 14 are placed on the mask surface 11, with each written stripe 14 displaced in the direction of the Y-axis the length of one scan line 14 (i.e., the written stripes 14 do not overlap).

In accordance with an embodiment of the present invention, multiple superimposed passes are used to create each written stripe 14. Each pass in a written stripe 14 has a different origin, such that patterns are exposed using an effective writing grid that is larger than the input pattern grid as will be discussed in detail below. In the preferred embodiment, eight superimposed passes are used. Advantageously, the present invention permits edge positioning with address-unit accuracy. Further, writing throughput is increased at small input pattern addresses.

Fig. 2 illustrates a particle beam lithographic system 30 utilizable for accomplishing the above writing technique. Lithographic system 30 includes a

particle or electron source 32, a beam modulating or blanking unit 34 for providing the modulation of the beam, a beam deflection and focus unit 36, a work chamber 38 containing the stage 40 with a work piece 42, which includes a layer of resist, and a means for determining the registration of the beam at the proper coordinates 44, all under the control of control equipment 46. This system is similar to the prior art systems of the Collier et al. and Lin patent disclosures, but uses the writing strategy in accordance with the present invention. It should be understood that lithographic system 30 may use particle beams, such as electron beams or ion beams. Of course, other lithographic systems that use, e.g., light, may be used if desired. Further, it should be understood that lithographic system 30 may operate on any desired work piece 42, which for ease of reference will be referred to herein as a mask.

Fig. 3 shows an input pattern grid 102 with superimposed writing grid 104 and effective writing grid 106, which are used in accordance with an embodiment of the present invention. As shown in Fig. 3, the input pattern grid 102 is illustrated as a series of cells, each representing an input address unit. The input pattern address size 103 is defined as the spacing between adjacent elements in input address grid 102. The input pattern data is centered in each cell of the input pattern grid 102, with the origin (0,0) of the input pattern data being the lower left of the grid, for illustration purposes. The input pattern address size 103 is, e.g., approximately 17.1875 nm, while the system operates at, e.g., 320 MHz. Of course, the address size 103 may be altered if desired, along with a corresponding change in frequency. Thus, for example, if a larger address size is used, e.g., approximately 34.375 nm, the operating system may operate at 160 MHz.

The writing pixels 108, i.e., the individual beam placement on the mask surface, occur at the vertices of the input pattern grid 102, i.e., offset by one-half an address unit from the pattern data grid, as indicated by the dots in Fig. 3. There are eight superimposed passes used in accordance with an embodiment of the present invention. Each pass uses a different origin defined by an offset. The number of the pass associated with each pixel is located in the cell adjacent the

writing pixel. Thus, as shown in Fig. 3, each of the eight passes is offset, in address units, as follows:

Pass Number	Offset
Pass 1	x=0.5, y=0.5
Pass 2	x=0.5, y=4.5
Pass 3	x=4.5, y=0.5
Pass 4	x=4.5, y=4.5
Pass 5	x=2.5, y=2.5
Pass 6	x=2.5, y=6.5
Pass 7	x=6.5, y=2.5
Pass 8	x=6.5, y=6.5

Table 1

The writing grid 104 is the array defined by the center-to-center distance between pixels produced during a single pass. Thus, as shown in Fig. 3, eight superimposed writing grids are shown, where each grid is defined by the number associated with the pass. The writing grid size 105 is the distance between scan lines 14 in the X-axis direction (direction of stage motion), and is also the theoretical pixel spacing in the Y-axis direction (direction of the scan motion). However, because the Y-axis scan is analog and not step-like, a pixel will typically not be a perfect spot but will be somewhat oblong in the direction of the continuous scan, i.e., the Y-axis. Thus, the writing grid size 105, in accordance with an embodiment of the present invention, is eight times the input address size 103. As shown in Fig. 3, after all passes are complete, a staggered checkerboard pattern is created.

In one embodiment, each of the eight passes is exposed completely before a subsequent pass is performed. As can be seen in Fig. 3, however, the pixels associated with the first pass and the second pass are positioned at the same X-axis location. Thus, in an alternative embodiment, the lithography system may perform two overlapping scans lines at each X-axis location prior to the stage 10 moving the scan to the next X-axis location. In another embodiment, pixels that are

located along the same scan line, i.e., pass 1/pass 2, pass 3/pass 4, etc., may be exposed during the same scan line. In this case, the writing grid size is four times the input address size 103. Both the scan lines 14 and the written stripes 14 may be produced with either uni-directional or bi-directional passes.

The effective writing grid 106 is the array defined by the pixels on the mask surface 11 after completion of all the passes in a single written stripe 14. After all passes, eight effective writing grid 106 sites, which are the same as pixels 108, fall into each 8x8 region of the input pattern grid 102. The effective writing grid size 107 is defined as the distance between rows or columns in the grid. Thus, in accordance with an embodiment of the present invention, the effective writing grid size 107 is two times the input address size 103. Note, however, that the distance to the nearest neighbor within the effective writing grid 106 is $2\sqrt{2}$. The staggered checkerboard writing grid 104 pattern advantageously fits the effective writing grid 106 uniformly over the input pattern grid 102.

The Gaussian spot size, i.e., diameter, of each pixel, as well as the dose of the beam, can be freely varied within the operating envelope of the system. It has been found that the spot size, i.e., the full width half maximum of the beam current distribution at the mask plane, may be approximately eight to nine times the input address size 103 to produce good lithography results. Thus, a spot to writing grid size 105 ratio of ≥ 1.00 provides adequate resolution. If forward scattering is considered, a smaller spot/grid ratio may be preferable for situations where the spot size approaches approximately 120nm.

The lithography system may perform at different blanking frequencies, determined by the size of the input address size. Thus, e.g., for input address sizes of less than or equal to 17.1875 nm, the system may operate at 320 MHz. However, for larger addresses, e.g., up to 34.375 nm, the system may operate at 160 MHz. Of course, if desired, the operating system may perform at 160 MHz for address sizes of less than or equal to 17.1875 nm.

The scan line exposure time is approximately 25.6 μs per scan line 16. Thus, at 320 MHz blanking operation with a 25.6 μs exposure time there are 8192 written pixels per scan line 16. The operating system pattern memory divides each

scan into 8 segments, 1024 bits per segment (320 MHz). For example, if the input address size is 15 nm, the stripe height is 8192 Pixels * writing grid size * 15 nm = 983040 nm (983 μm). Of course, a lithography system with different exposure times, blanking frequencies and pixels per scan line may be used in accordance with an embodiment of the present invention.

The writing strategy in the Berglund et al. patent disclosure in U.S. Patent 5,103,101, which is incorporated herein by reference, uses multipass printing with four passes per written stripe. Thus, in Berglund et al. each input address is expressed as four pixels, with each pixel next to each other.

For the sake of comparison, Fig. 4 shows an address grid 110 illustrating the writing strategy used in U.S. Patent 5,103,101. The first pass is labeled "A", the second pass is labeled "B", the third pass is labeled "C" and the fourth pass is labeled "D". As can be seen in Fig. 4, the writing grid size 112, i.e., the center-to-center distance between like labeled pixels is equal to two times the input address size. The effective writing grid size 114, as taught in Berglund et al., however, is equal to the input address size 116. Thus, advantageously, the present invention provides a faster throughput, because not all input pattern grid locations must be exposed.

Because the writing grid size 105 is eight times the input address size 103, and the effective writing grid size is twice the input address size 103 in the present invention, throughput is increased compared to single pass printing by a theoretical maximum factor of eight ((writing grid size/input pattern size)^2/8=8) and by a factor of eight compared to the writing strategy of Berglund et al as depicted in Fig. 4. The present invention also has a theoretical throughput factor of two times that of the "virtual addressing" embodiment described in Berglund et al.

In accordance with an embodiment of the present invention, pattern data sampling is used to determine which pixels are exposed during each pass. Fig. 5 shows a sampling matrix 120 for sampling pattern data with horizontal and/or vertical edges. Only the pattern data located within the numbered and shaded locations of sampling matrix 120 are examined and all other data, i.e., information located in non-shaded cells, is ignored. Thus, the pattern to be printed is compared

with the sampling matrix 120 and, e.g., if there is any pattern data at location 1 in sampling matrix 120, then the corresponding adjacent writing pixel (indicated by dot 122) will be exposed during pass 1. The same rule holds true for locations 2 through 8 and passes 2 through 8. Conversely if there is no pattern data at locations 1 through 8, then the corresponding pixel is not exposed. The entire pattern data set is sampled in this manner using tiled sampling matrices. Sampling matrix 120 provides edge placement with input-pattern-file address-unit accuracy. This is particularly useful if pattern features are significantly larger than the size of the sampling matrix.

While sampling matrix 120 is chosen for accurate placement of horizontal and vertical edges, sampling matrix 120, however, introduces placement errors for angled edges. Accordingly, different sampling matrices are used for angled edges. Fig. 6 shows four sampling matrices 131, 132, 133, and 134 that may be used for angled edges. Each sampling matrix 131-134, shown in Fig. 6, is used for angled edges having different angles, as follows:

Matrix Number	Angle
Matrix 131	0.00° - <14.04° (aspect ratios 0 to ¼)
Matrix 132	14.04° - <36.87° (aspect ratios 1/4 to 3/4)
Matrix 133	36.87° - <45.00° (aspect ratios 3/4 to 1/1)
Matrix 134	45.00° - <53.13° (aspect ratios 1/1 to 4/3)
Matrix 132	53.13° - <75.96° (aspect ratios 4/3 to 4/1)
Matrix 131	75.96° - <90.00° (aspect ratios 4/1 to vertical)

Table 2

Sampling matrices 131-134 may be mirrored for angles greater that 90°.

In another embodiment, sampling matrix 120 is used for horizontal, vertical and angled edges. With use of only one sampling matrix, implementation is simplified. This embodiment may be particularly useful when small addresses are used. As noted above, alternative embodiments may overlap exposure during one scan line. The writing grid size must be adjusted accordingly.

Figs. 7, 8, 9A, 9B, and 10 illustrate the operation of sampling a geometric figure, storing the pattern data and printing the figure on a mask in accordance with an embodiment of the present invention. Fig. 7 shows, by way of an example, a portion of a geometric figure 150 that is to be printed on a mask. Geometric figure 150 includes a horizontal line defined by a section 152 of geometric figure 150 and a section 154 that is not to be printed on the mask or wafer (indicated by shading). It should be understood that geometric figure 150 is merely a portion of the image that is to be printed on a mask and that for accurate edge placement, the pattern should span approximately 3 writing grid sizes.

Fig. 8 shows a sampling matrix 160 that is used to sample the data in geometric figure 150. Sampling matrix 160, shown as is 32 x 16 address units in size, includes several tiled matrices 120. As described above in reference to Fig. 5, the only pixels to be printed are those with data information located in the cell adjacent the pixel (indicated by the number of the pass associated with the pixel). If geometric figure 150 included an angled edge, the appropriate matrix 131 through 134 may be used to sample the data of the angled edge.

The data in geometric data 150 is decomposed into eight phases, with one phase associated with each pass, using sampling matrix 160. Figs. 9A and 9B show the scan conversion of the geometric figure 150 into eight phases. The data conversion algorithm samples the geometric figure 150 and places into memory the pattern data. The scan conversion algorithm for the first phase places into pattern memory only those pixels where the pattern data from geometric figure 150 is found at location 1 in sampling matrix 160. This is indicated in Figs. 9A and 9B by grid 171. The pixels that are to be printed are labeled with a numeral "1" in grid 171. The "1" pixels can then written on a bit map 181, which may held in a data buffer. Because bit map 181 is used for phase 1 pixels, bit map 181 is much smaller than the entire sampling matrix, e.g., shown as 4 x 2 address units in size.

Similarly, the scan conversion algorithm for the second through eighth phases determines where the pattern data from geometric figure 150 is found in the sampling matrix 160 as indicated by grids 172-178, respectively. The pixels that are to be printed are shown labeled with numerals that correspond with the phase

number and location in the sampling matrix 160. The pixels can then be written on bit maps 182-188

In one embodiment, these processes are part of a single software transformation done for each phase. The information in the bit maps 181-188 in the data buffer, which may be, e.g., shift registers, is transferred to the raster scan lithography system 190, shown in Fig. 10, which exposes the sensitive surface 192 with the composite pixel pattern 194. A single bit map data buffer is quite large and each phase is completed before the next is begun. It should be obvious that, the size of the bit map buffers 181-188 are not fundamental to the invention. It should also be obvious that the portion of each phase completed before another phase is begun is also not important as long as the composite pixel pattern 194 is completely exposed on the sensitive surface 192.

When the desired writing on the resist is complete, the resist is processed by conventional lithographic development techniques resulting in features as defined by the pixels during writing.

Offset scan voting may be used in accordance with an embodiment of the present invention. For offset scan voting, each of the eight passes is written physically offset by 1/8 of a writing stripe. The intent is to average uncorrectable components of scan linearity and stage positioning. Because of this physical offset, the exposure data must also be offset for each pass, to ensure proper overlay of the printed phases. The segments of pattern memory are loaded in such a way that a substrate stripe is exposed by pixels that originate from a different section of the operating system's scan line on each pass. In the Y direction, the N^{th} pass (phase) starts at (N-1)*(stripe height)/8; N = 1 … 8.

Offset scan voting (eight pass) is shown schematically in Fig. 11. For clarity, the eight passes, in reality superimposed, are shown displaced horizontally. Each shade corresponds to one region on the mask. The eight written stripe regions are labeled *a-h* (this periodic labeling repeats in the Y direction). Eight contiguous segments of pattern memory are labeled *1-8*. After each pass, the stage is translated in the Y direction $1/8^{th}$ of a written stripe height before the next pass. Thus, each stripe region is exposed by eight different sections of pattern memory.

As exceptions, stripes at the bottoms and top of the pattern area, for example, (a,1) must be computed and written differently, to provide full dose to the sensitive surface. For example, the bottom stripe may be computed by assuming that there are stripes below the bottom strip, which are not written. Thus, the proper computation and dosage for the bottom stripe may be computed and written. The top stripe is computed and written in a similar manner as will be well understood by those skilled in the art. Note that eight distinct pairings of stripe region (*a-h*) and pattern memory (*1-8*) are used for the full exposure.

Although the present invention is illustrated in connection with specific embodiments for instructional purposes, the present invention is not limited thereto. Various adaptations and modifications may be made without departing from the scope of the invention. Accordingly, all such changes come within our invention.

CLAIMS

What is claimed is:

1. In the generation of a pattern in a raster scan lithography system, the steps comprising:

forming a beam of a predetermined diameter defining the width of a pixel of the pattern;

providing a material sensitive to said beam to be irradiated by the beam;

forming a plurality of said pixels by directing said beam onto said material;

controlling said beam as it forms said pixels to form an array of pixels, each pixel being an element of a feature of the pattern; and

repeating the steps of forming and controlling a plurality of times, with each step forming a separate array of pixels, each pixel being an element of a predefined feature not formed in a previous step of forming such that the composite of all steps of forming forms a staggered grid array of pixels that define a feature of the pattern.

2. The method of Claim 1, further comprising sampling the pattern with a sampling matrix having an array of cells of a predetermined address size, and wherein said staggered grid array of pixels forms a plurality of columns, said plurality of columns being separated by a distance that is greater than the predetermined address size.

3. The method of Claim 2, wherein said plurality of columns are separated by a distance that is twice the predetermined address size.

4. The method of Claim 2, wherein each of said separate array of pixels has a size that is greater than the distance separating said plurality of columns.

5. The method of Claim 4, wherein said array of pixels has a size that is eight times said predetermined address size.

6. The method of Claim 2, wherein sampling the pattern with a sampling matrix having an array of cells of a predetermined address size, comprises sampling the pattern with a first sampling matrix when said pattern has horizontal and vertical features and sampling the pattern with at least a second sampling matrix when said pattern has an angled feature.

7. The method of Claim 6, further comprising sampling the pattern with one of a plurality of sampling matrices when said pattern has an angled feature, wherein selecting said one of a plurality of sampling matrices is based on the angle of said angled feature.

8. The method of Claim 2, wherein each pixel has a spot size that is at least approximately eight times the predetermined address size.

9. The method of Claim 1, wherein each separate array of pixels is offset by a different amount.

10. The method of Claim 1, wherein the step of repeating includes repeating seven times, thereby forming said pattern in eight passes.

11. The method of Claim 1, wherein said beam is one of an electron beam, light beam, and ion beam.

12. The method of Claim 1, wherein controlling said beam includes offset scan voting.

13. A raster scan system for forming a pattern on a radiation sensitive material, said system comprising:

means for forming a radiation beam of a predetermined diameter defining the width of a pixel of the pattern;

means for forming a plurality of said pixels by directing said beam onto said material;

means for controlling said beam as it forms said pixels to form an array of pixels, each pixel being an element of a feature of the pattern; and

means for repeating the forming of said pixels by passing said beam across said material a plurality of times, with each pass forming a separate array of pixels, each pixel being an element of a predefined feature not formed in a previous pass, such that passes together form a staggered grid array of pixels that define a feature of the pattern.

14. The raster scan system of Claim 13, further comprising means for sampling the pattern with a sampling matrix having an array of cells of a predetermined address size, and wherein said staggered grid array of pixels forms a plurality of columns, said plurality of columns being separated by a distance that is greater than the predetermined address size.

15. The raster scan system of Claim 14, wherein said means for sampling the pattern with a sampling matrix comprises a means for sampling the pattern with a first sampling matrix when said predefined feature is horizontal or vertical and for sampling the pattern with a second sampling matrix when said predefined feature is at an angle.

16. In the generation of a raster scan pattern, the steps comprising:

forming a beam of a predetermined diameter defining the width of a pixel of the pattern;

providing a material sensitive to said beam to be irradiated by the beam;

forming a plurality of said pixels by directing said beam onto said material;

controlling said beam as it forms said pixels during a first pass to form an array of pixels in a writing grid over an area of said material, each pixel being an element of a feature of the pattern, the writing grid having a predetermined size; and

repeating the steps of forming and controlling a plurality of times to form a plurality of arrays of pixels in a plurality of writing grids in subsequent passes over said area of said material, each writing grid being offset by a different amount, such that the composite of all writing grids forms an effective writing grid, the predetermined size of the writing grid being at least four times greater than the size of the effective writing grid defined by the distance between adjacent columns of pixels.

17. The method of Claim 16, further comprising sampling the pattern with a sampling matrix having an array of cells of a predetermined address size, said effective writing grid being at least twice the predetermined address size.

18. The method of Claim 17, wherein said array of cells includes columns and rows, said pattern is sampled once every eight columns and once every eight rows.

19. The method of Claim 16, wherein a total two to four passes are performed over said area of said material.

20. The method of Claim 17, wherein the width of said pixel is at least approximately eight times the predetermined address size.

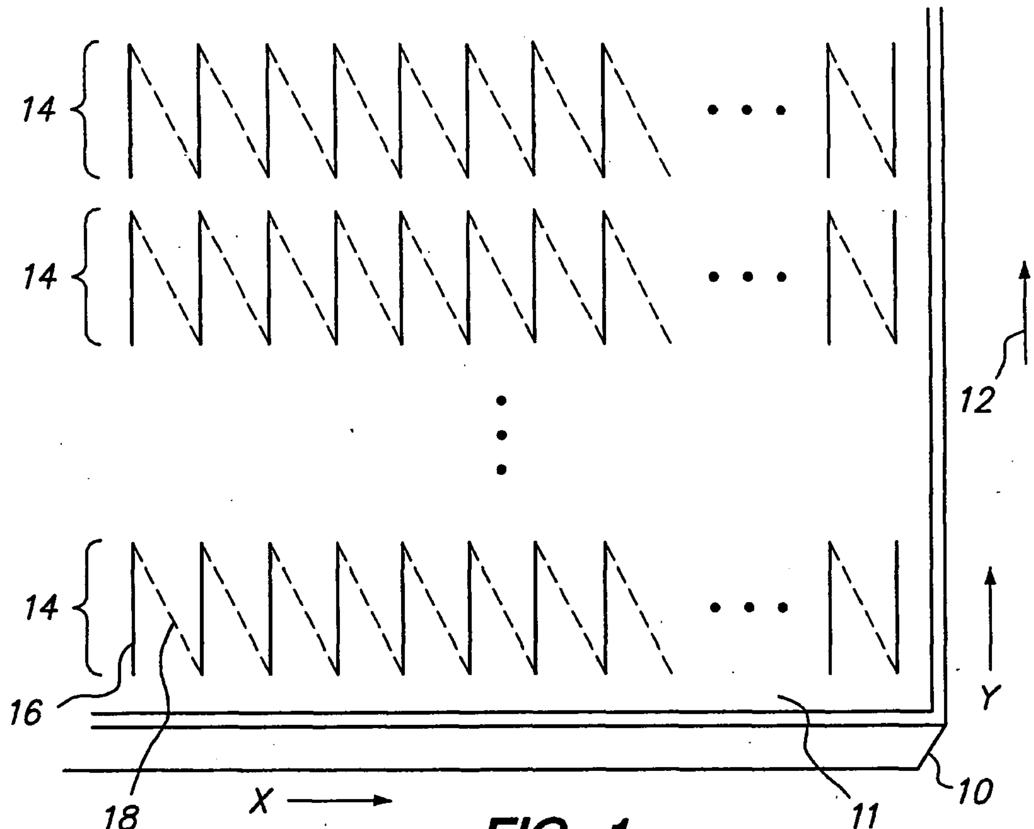
14
14
14
16
18
X
Y
12
11
10

FIG. 1

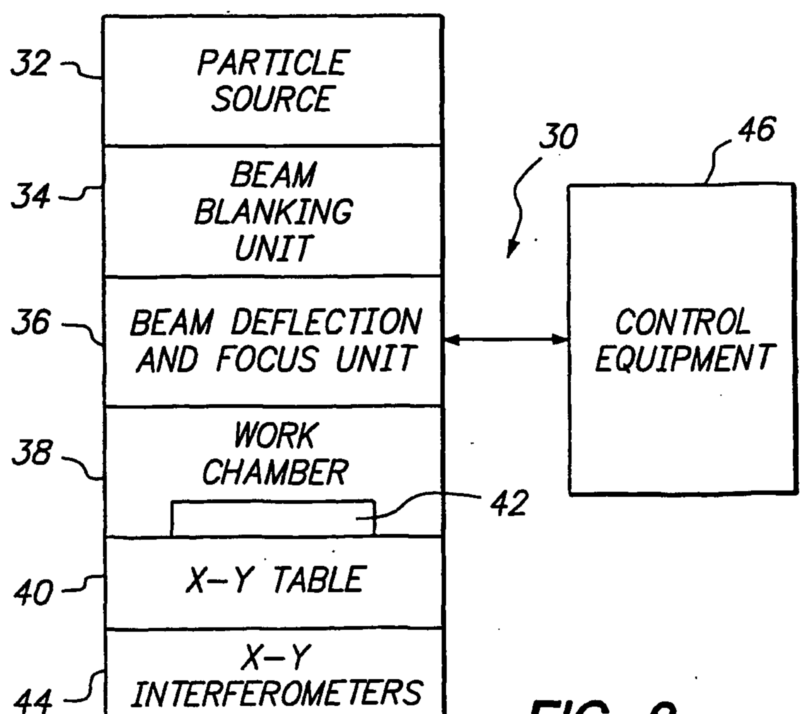
32
PARTICLE SOURCE
34
BEAM BLANKING UNIT
36
BEAM DEFLECTION AND FOCUS UNIT
38
WORK CHAMBER
42
40
X-Y TABLE
44
X-Y INTERFEROMETERS
30
46
CONTROL EQUIPMENT

FIG. 2

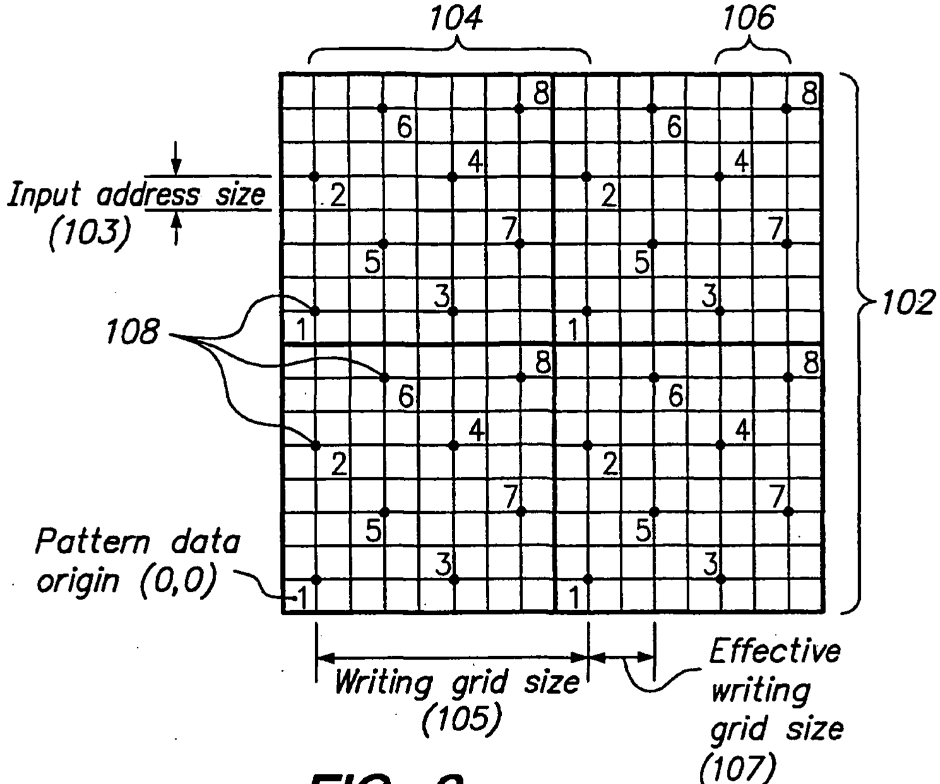

FIG. 3

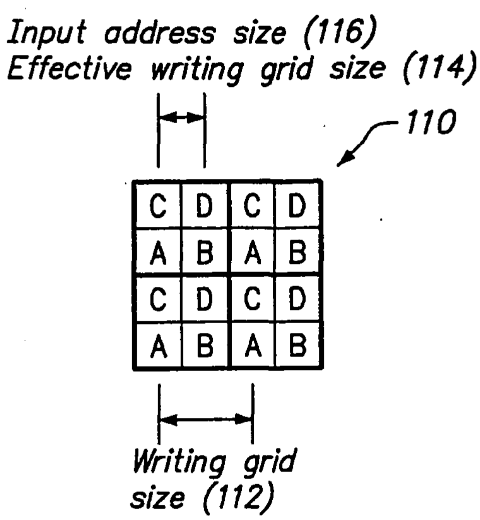

FIG. 4
(PRIOR ART)

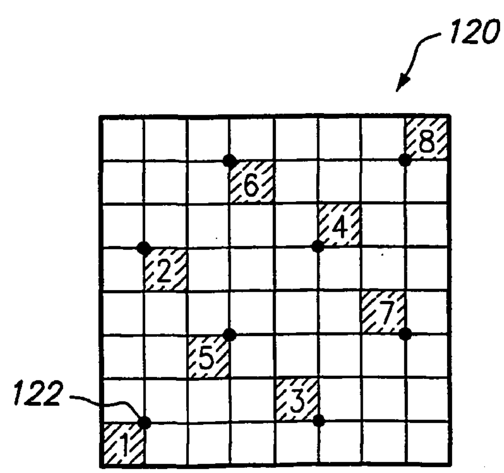

FIG. 5

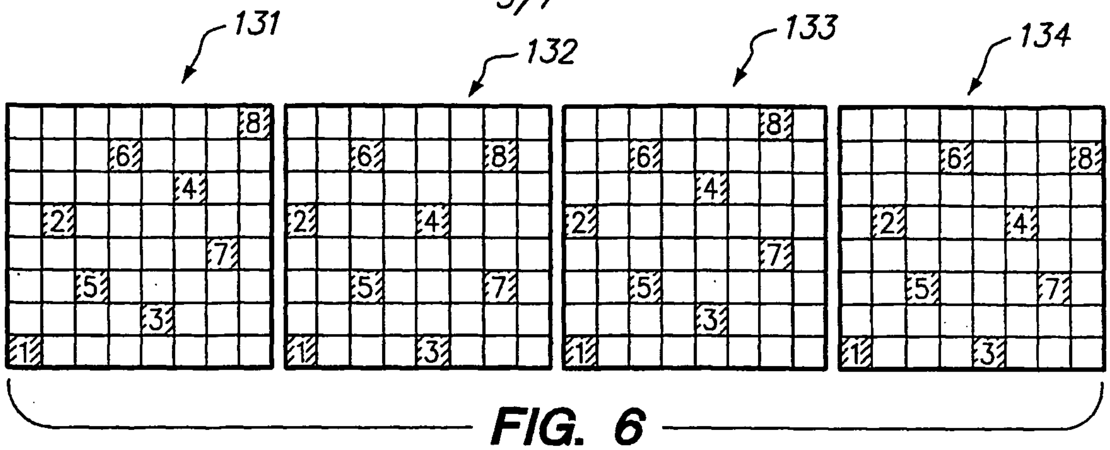

FIG. 6

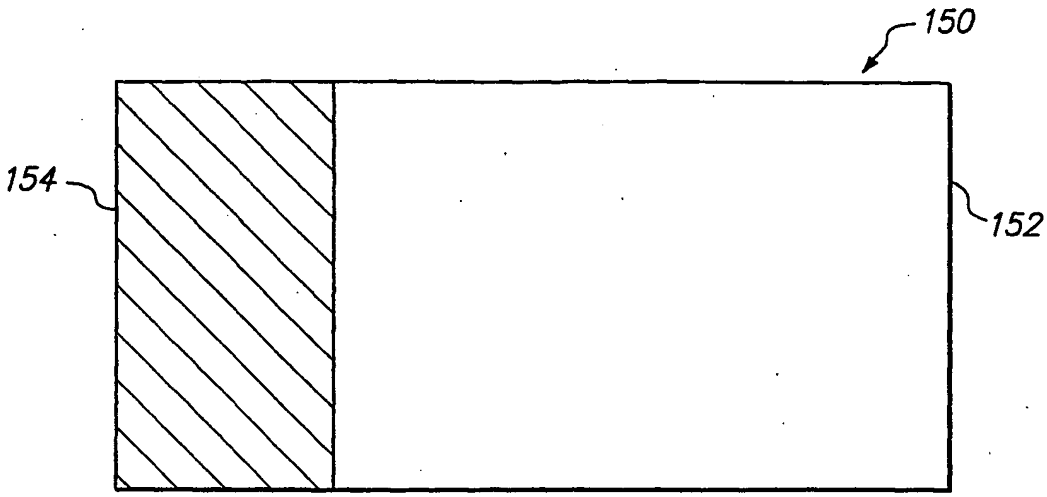

FIG. 7

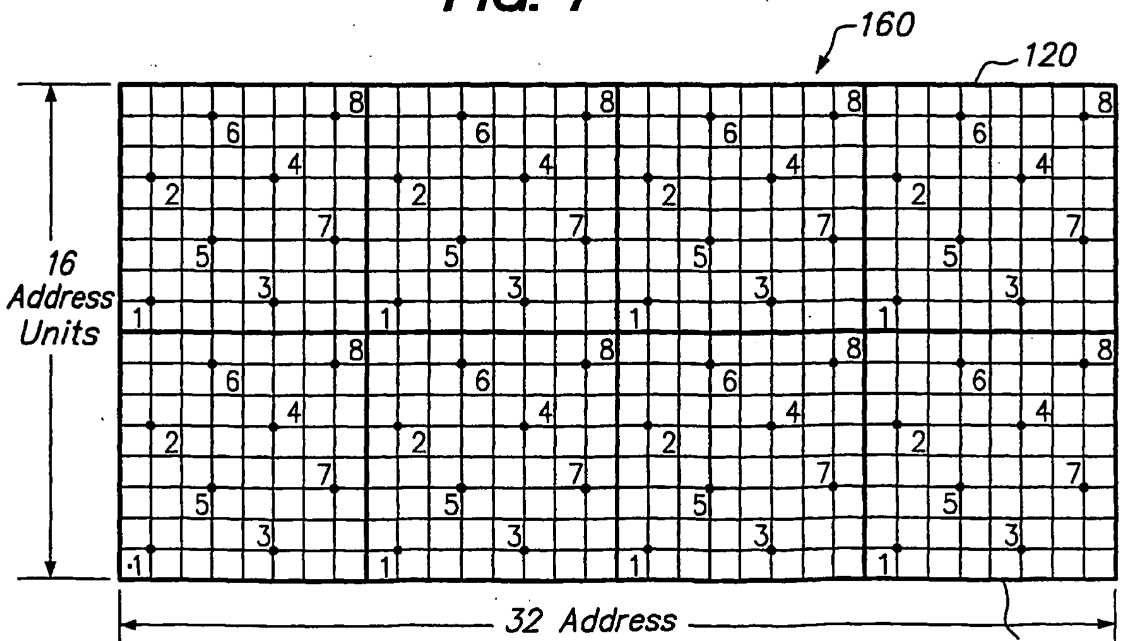

FIG. 8

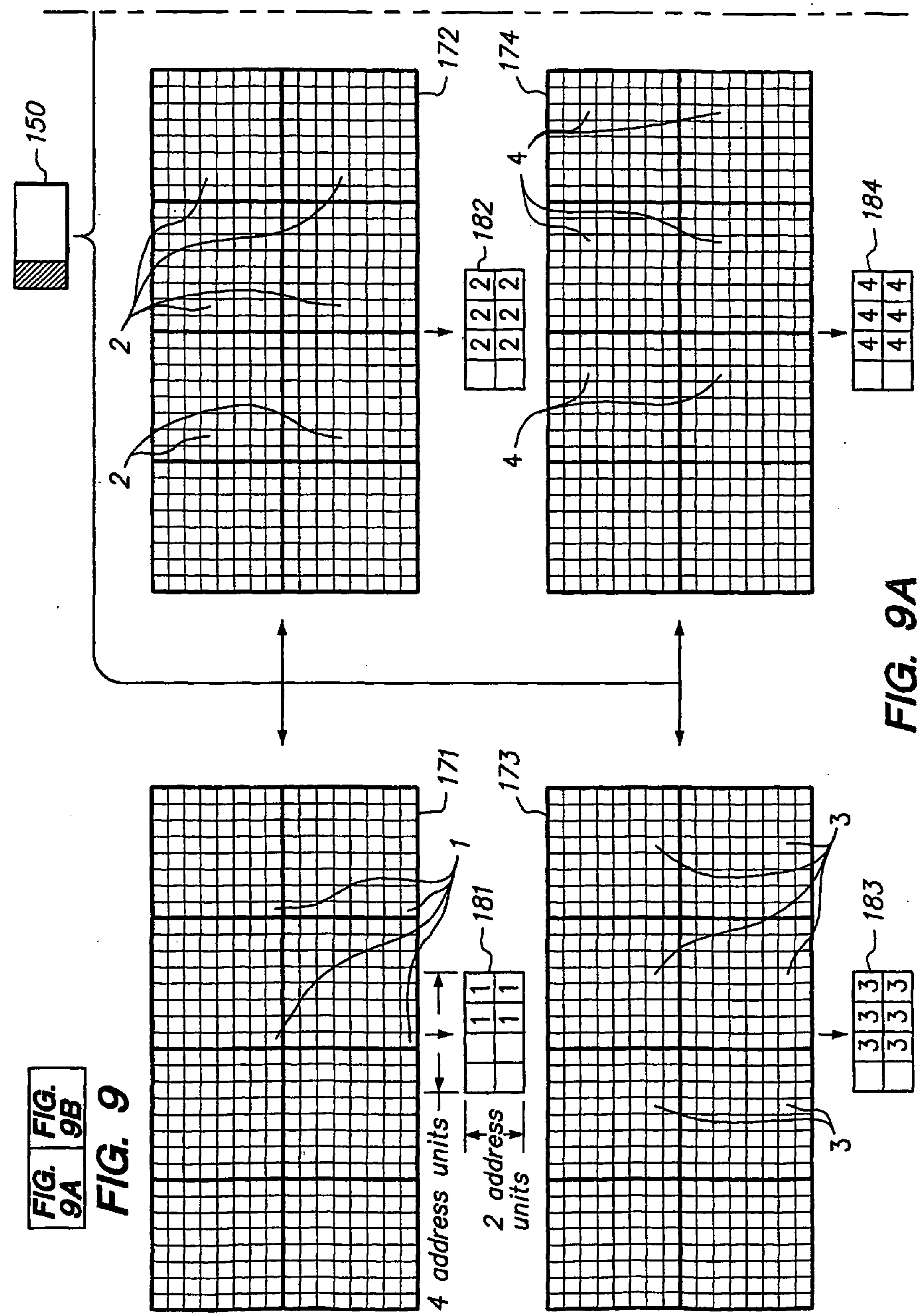
150
172
174
171
173
182
184
181
183
4 address units
2 address units
FIG. 9A
FIG. 9B

FIG. 9

FIG. 9A

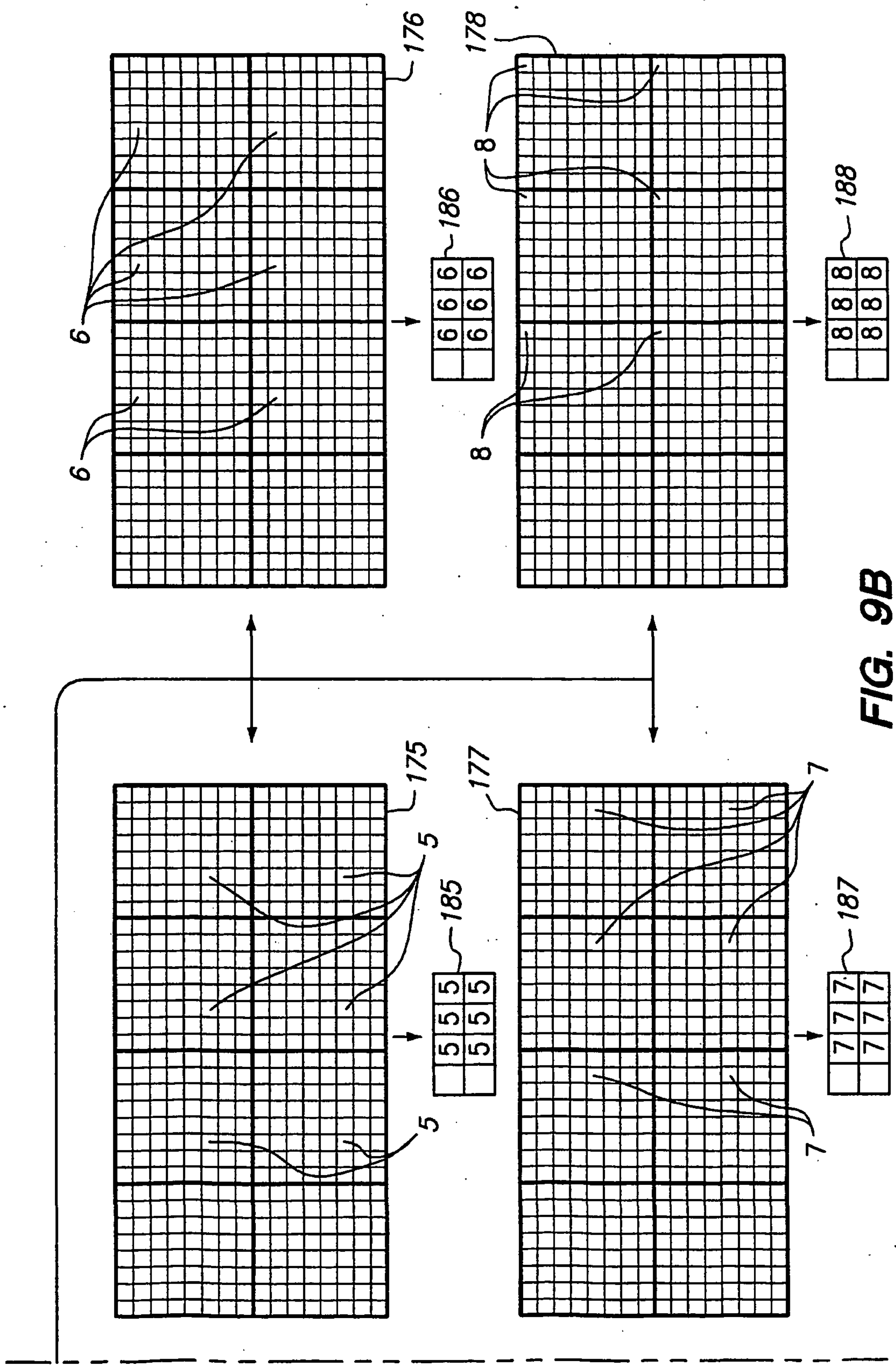

FIG. 9B

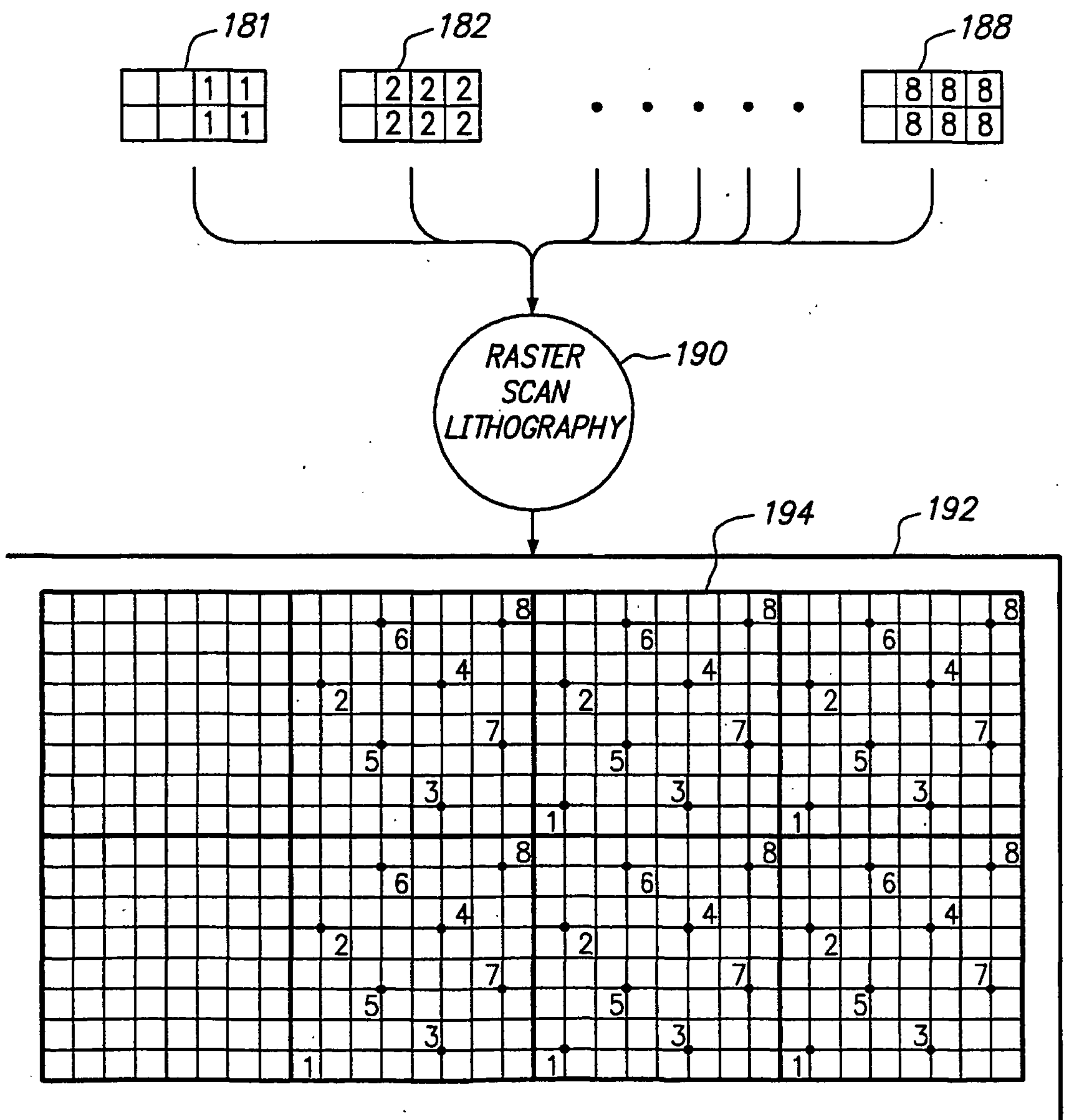
181
182
188
1 1
1 1
2 2 2
2 2 2
8 8 8
8 8 8
RASTER SCAN LITHOGRAPHY
190
194
192
8
6
4
2
7
5
3
1

FIG. 10

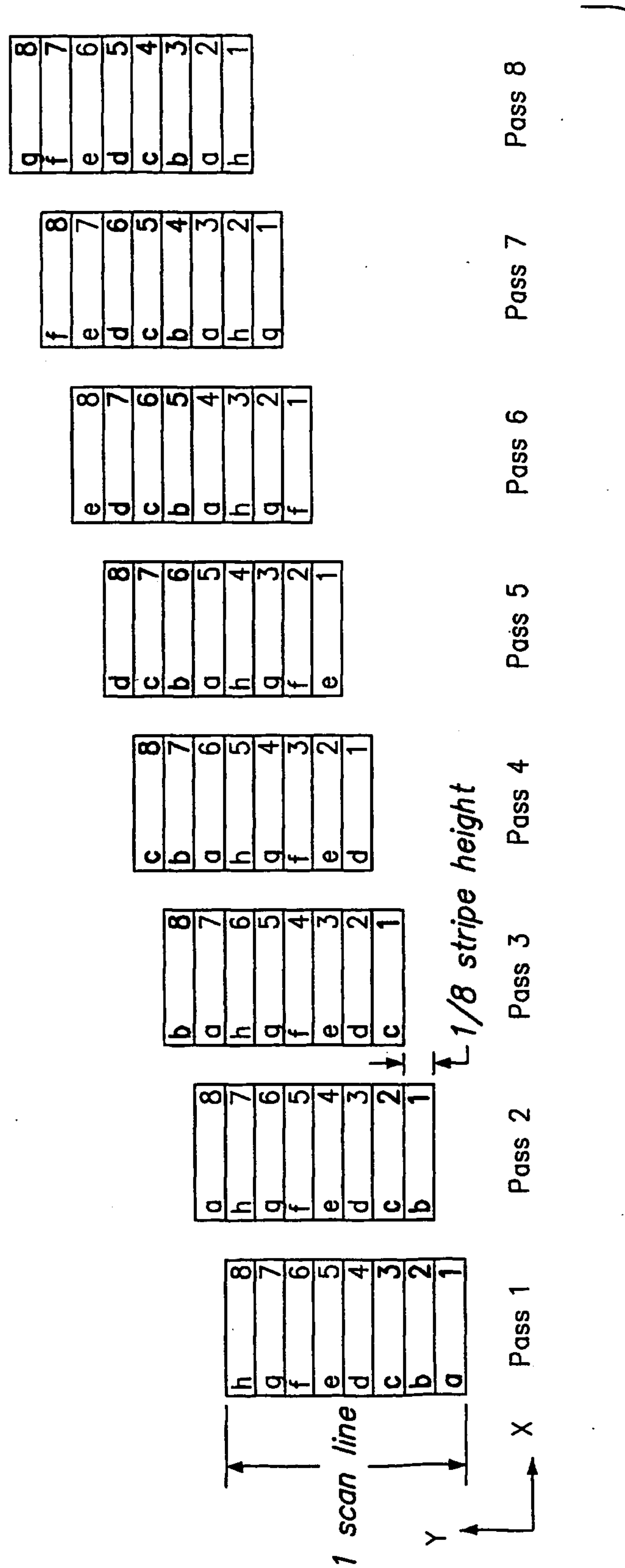
Pass 1
Pass 2
Pass 3
Pass 4
Pass 5
Pass 6
Pass 7
Pass 8
1 scan line
1/8 stripe height
X
Y

FIG. 11